Characterization of MOS transistors integrated on high-resistivity silicon with a DSSD process (*)

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Summary. — We have fabricated MOS transistors with a commercial double-sided silicon detector (DSSD) process, on the same wafer as the detector. These devices have been simulated and measured in the lab both in the DC characteristics and in the noise figures.

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1. - Introduction

Present and future silicon trackers for high-energy physics experiments call for an ever increasing electronic readout density. Integrating some part of the preamplifier on the silicon detector substrate would open huge areas and change the design paradigm for such systems. In particular, integration of a proper circuit on the detector substrate allows a better coupling between the strips and the electronic readout. Other groups have tackled this problem in the past, developing ad-hoc detector processes to optimize the performance of the MOS devices. For instance Holland [1] has developed a special high-temperature detector process with a gettering layer on the back side that yields both low leakage current and good MOS transistors. This process is not easily applied to double-sided detectors.

Our approach to the problem is to use a mature double-sided process and integrate the MOS devices using what is available in the process. In this way we could minimize development costs and still have usable devices.

2. - Process and electrical simulation

We have employed a by now commercial DSSD process [2] that our group has developed with the CSEM foundry in Neuchâtel, Switzerland. The process has p and n
implants on both sides of the wafer and the readout strips are AC coupled to the charge collecting implant through a dielectric formed by a layer of SiO₂ and a layer of Si₃N₄. We use this 300 nm thick dielectric as gate oxide for the MOS devices. The gate itself is made of n-doped polysilicon, while the substrate is 8 kΩcm, (111), n-type silicon. To limit production costs, no changes were introduced in the detector process, making our transistors 100% compatible with high-quality detectors. The process simulations (on both sides of the wafer) were performed with the ISE-tCAD dios tool [3]. By means of a process description in a text file, the dios tool simulates the process steps obtaining a device (MOS transistor) section. We have extracted the doping profiles for drain and source implants and the effective value for channel length. Results for both junction and ohmic sides are shown in fig. 1 and table I, where \( x_{\text{peak}} \) is the depth for maximum doping value, \( N_{\text{a peak}} \) is the boron doping value at \( x_{\text{peak}} \), \( x_{\text{junc}} \) is junction depth, \( x_{\text{lat}} \) is the p⁺ implant lateral diffusion and \( R_{\text{sheet}} \) is the p⁺ implant sheet resistance.

We note a difference for the peak value due to a different dose of the boron implant on the two sides. The sheet resistance values obtained by simulated profiles agree with the measured values on the Van der Paw structures integrated on the wafer. This agreement allows us to use the doping profiles in electrical simulations of MOS transistors. Full electrical simulations were performed with the ISE-tCAD dessis tool which allows us to trace input and output DC characteristics. Simulations and measurements are shown later.

**Table I.** Doping characteristics.

<table>
<thead>
<tr>
<th></th>
<th>J-side</th>
<th>Ω-side</th>
</tr>
</thead>
<tbody>
<tr>
<td>( x_{\text{peak}} )</td>
<td>0.11 ( \mu \text{m} )</td>
<td>0.1 ( \mu \text{m} )</td>
</tr>
<tr>
<td>( N_{\text{a peak}} )</td>
<td>( 1.92 \times 10^{19} \text{ cm}^{-3} )</td>
<td>( 5.22 \times 10^{18} \text{ cm}^{-3} )</td>
</tr>
<tr>
<td>( x_{\text{junc}} )</td>
<td>0.8 ( \mu \text{m} )</td>
<td>0.8 ( \mu \text{m} )</td>
</tr>
<tr>
<td>( x_{\text{lat}} )</td>
<td>0.7 ( \mu \text{m} )</td>
<td>0.7 ( \mu \text{m} )</td>
</tr>
<tr>
<td>( R_{\text{sheet}} )</td>
<td>300 Ω/square</td>
<td>2.8k Ω/square</td>
</tr>
</tbody>
</table>
3. MOS capacitors

We have characterized the Si-SiO₂ interface and the dielectric layer through measurements and models on MOS capacitors. We have integrated two different types of MOS capacitors, a thin oxide and a thick oxide one (see fig. 2). Both have 200 nm of SiO₂ and 120 nm of Si₃N₄ dielectric layers and, for the thick oxide capacitor, a further 700 nm LTO oxide is present; for a good understanding of Si-SiO₂ interface properties we need to measure both MOS capacitors. We obtain a measure of MOS capacitor characteristics by means of a high-frequency C-V curve; however, high-resistivity silicon limits the maximum value for the measuring frequency. To understand this...
problem we measure $C_s$ and $R_s$ (series capacitance and resistance) for a MOS capacitor biased in the accumulation region. In this region the MOS capacitor small-signal model is shown in fig. 3a); $C_{ox}$ is the capacitance of dielectric layer, $R_{bulk}$ is the bulk resistance and $C_{bulk}$ is the bulk capacitance. From CSEM process data we can calculate $C_{ox}$, $C_{bulk}$ and $R_{bulk}$. For thin and thick oxide MOS capacitors we have:

$A = 3 \times 10^{-6} \text{m}^2$ (capacitor area),
$t_{ox} = 260 \text{ nm (equivalent } t_{SiO_2}, \text{ thin oxide)},$
$t_{ox} = 960 \text{ nm (equivalent } t_{SiO_2}, \text{ thick oxide),}$
$w_{Si} = 300 \mu \text{m (wafer thickness)},$
$q = 8 \text{k}\Omega \text{cm (bulk resistivity);}$

we obtain

$C_{ox} = 393 \text{ pF (thin oxide),}$
$C_{ox} = 107 \text{ pF (thick oxide),}$
$C_{bulk} = 1 \text{ pF ,}$
$R_{bulk} = 8 \text{ k}\Omega.$

Expressing the AC model parameters $C_s$ and $R_s$ as functions of $C_{ox}$, $C_{bulk}$ and $R_{bulk}$ we obtain

\begin{equation}
C_s = \frac{C_{ox}}{1 + \frac{C_{ox}}{C_{bulk}} \frac{\alpha_{bulk}}{1 + \alpha_{bulk}}},
\end{equation}

\begin{equation}
R_s = \frac{R_{bulk}}{1 + \alpha_{bulk}},
\end{equation}

where $\alpha_{bulk} = \omega^2 C_{bulk}^2 R_{bulk}^2$ and $\omega = 2\pi f$. For the thin oxide capacitor, in the low-frequency region, $C_s = C_{ox}$ when $f < 1 \text{ MHz},$ while $R_s = R_{bulk}$ when $f < 20 \text{ MHz}. To limit the error on $C_{ox}$ to 1%, we need to limit the measuring frequency to 100 kHz. Using the
model in fig. 3a) on the thin oxide MOS capacitor we obtain the curves shown in fig. 4. The measurements present differences with respect to the model. The measured $R_{\text{bulk}}$ is significantly lower than the expected 8 kΩ, because of a spreading current effect to the back and the $C_s$ capacitance has a lower corner frequency. To understand the differences between the measurement and the model for thin oxide MOS capacitor we analyse the physical structure. If we suppose a bad contact between the metal layer and polysilicon gate, the model for this structure is shown in fig. 3b). In fig. 5 measurements and model are superimposed, showing excellent agreement. This problem limits the maximum value for the frequency to 10 kHz in tracing the high-frequency C-V curve; this limitation leads to an error in the interface charge ($N_f$) calculation owing to incomplete disactivation, at this frequency, of interface trapped charge. We can use the thin oxide MOS for oxide thickness measurement, while for the interface charge calculation we need the thick oxide MOS capacitor. Since the first SiO₂ layer is the same in both capacitors we expect this $N_f$ determination to be accurate. The measurement yields the following results shown in table II.

### Table II. Thin oxide MOS capacitor; typical values.

<table>
<thead>
<tr>
<th></th>
<th>J-side</th>
<th>Ω-side</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{ox}$ (pF)</td>
<td>380</td>
<td>372</td>
</tr>
<tr>
<td>$t_{ox}$ (nm)</td>
<td>271</td>
<td>277</td>
</tr>
<tr>
<td>$N_f$ (cm⁻²)</td>
<td>$1.43 \times 10^{11}$</td>
<td>$1.36 \times 10^{11}$</td>
</tr>
<tr>
<td>$V_{th}$ (V)</td>
<td>-2.37</td>
<td>-2.27</td>
</tr>
</tbody>
</table>

4. MOS transistors

PMOS and NMOS devices with nominal design widths and lengths shown in table III have been fabricated. Measurements and simulations were performed to understand the basic functionality of the devices and the correctness of the simulation. A process problem has prevented the proper fabrication of NMOS devices, therefore
TABLE III. – MOS transistors dimensions.

<table>
<thead>
<tr>
<th>L (μm)</th>
<th>w (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>4, 8, 20, 40, 80</td>
</tr>
<tr>
<td>6</td>
<td>6, 12, 30, 60, 120</td>
</tr>
</tbody>
</table>

Fig. 6. – J and Ω side PMOS transistors.

only PMOS devices are discussed here. A cross-section for PMOS transistors on
junction and ohmic side is shown in fig. 6. For PMOS devices we have measured the
DC input and output characteristics, the small signal parameters $g_m$ and $r_d$ and the
noise spectrum.

A) Input characteristics

$I_d$ vs. $V_{gs}$ ($V_{ds} = -0.1$ V) measurement and simulation are shown in fig. 7 for a
PMOS 120/6 transistor at 0 V back voltage. The simulation uses the $N_f$ value found from
the MOS capacitor. In tables IV and V we show the typical values for the PMOS threshold voltages on both sides, for different widths and channel lengths.

We have also investigated the influence of the narrow and short channel effects.
For a MOS transistor on high-resistivity silicon, source and drain depletion regions are
in the range of tens of μm; the narrow channel effect appears for a channel width below
20 μm (see table IV and V). A short channel effect is present; the source and drain
depletion regions extend below the whole channel and the electric field is not
perpendicular to gate; a smaller $V_{th}$ is necessary to switch on the channel. However this
reduction is negligible compared with the $V_{th}$ value. For a PMOS transistor the
expression for the threshold voltage is [4]

$$ V_{th} = V_{fb} - 2 \psi_B - \frac{Q_d}{C_{ox}}, $$

(3)
Fig. 7. – PMOS 120/6 J-side input characteristics.

**TABLE IV.** – L = 6 μm typical threshold voltage (V_{back} = 0 V).

<table>
<thead>
<tr>
<th>w (μm)</th>
<th>V_{th} (J-side)</th>
<th>V_{th} (Ω-side)</th>
</tr>
</thead>
<tbody>
<tr>
<td>120</td>
<td>-2.15 V</td>
<td>-2.13 V</td>
</tr>
<tr>
<td>60</td>
<td>-2.17 V</td>
<td>-2.14 V</td>
</tr>
<tr>
<td>30</td>
<td>-2.22 V</td>
<td>-2.16 V</td>
</tr>
<tr>
<td>12</td>
<td>-2.38 V</td>
<td>-2.23 V</td>
</tr>
<tr>
<td>6</td>
<td>-2.75 V</td>
<td>-2.37 V</td>
</tr>
</tbody>
</table>

**TABLE V.** – L = 4 μm typical threshold voltage (V_{back} = 0 V).

<table>
<thead>
<tr>
<th>w (μm)</th>
<th>V_{th} (J-side)</th>
<th>V_{th} (Ω-side)</th>
</tr>
</thead>
<tbody>
<tr>
<td>80</td>
<td>-2.37 V</td>
<td>-2.12 V</td>
</tr>
<tr>
<td>40</td>
<td>-2.27 V</td>
<td>-2.16 V</td>
</tr>
<tr>
<td>20</td>
<td>-2.37 V</td>
<td>-2.27 V</td>
</tr>
<tr>
<td>8</td>
<td>-2.60 V</td>
<td>-2.31 V</td>
</tr>
<tr>
<td>4</td>
<td>-2.95 V</td>
<td>-2.35 V</td>
</tr>
</tbody>
</table>

where \( V_{fb} \) is the flat-band voltage, and \( Q_d \) the depletion layer charge:

\[
\Psi_B = \frac{kT}{q} \ln \left( \frac{N_d}{n_i} \right),
\]

\[
Q_d = \sqrt{2\varepsilon_S q N_d \left( 2\Psi_B + |V_{SB} | \right)}.
\]

The short-channel effect decreases the \( Q_d \) value, which however is already small owing to a low \( N_d \) value for the bulk doping. Therefore, for a MOS transistor on high-resistivity silicon, the short-channel effect does not change much the value of the threshold voltage; the flat-band voltage, strictly connected to the \( N_f \) value, gives the dominant contribution.
B) Body effect

This effect gives a dependence of $V_{th}$ on the reverse bias between source and bulk; the reverse back-side voltage affects the carrier density in the channel. In particular, for a PMOS transistor, the absolute value of the threshold voltage increases with increasing back voltage. Figure 8 shows $V_{th}$ vs. $V_{sb}$ for PMOS 120/6 on junction and ohmic side.

On the junction side we have roughly a dependence of $V_{th}$ on the square root of $V_{sb}$. On the ohmic side we have a different behaviour. In fact a negative bias to the backside extends the p$n$ (back-bulk) depletion region toward the channel zone. Carriers under the channel will not change until the depletion region reaches the ohmic side and from now on the effect of depletion will affect carrier density and threshold voltage. On both sides, the low doping value limits $V_{th}$ vs. $V_{sb}$ variations; this is a significant feature for a transistor which should work on the same substrate as the detector.

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**Figure 8.** $V_{th}$ vs. $V_{sb}$ for PMOS 120/6 on junction and ohmic side.

**Figure 9.** PMOS 120/6 J-side output characteristics; $V_{sb} = 0$; markers = measurement.
Fig. 10. – PMOS 120/6 Ω-side output characteristics; $V_{sb}=0$; markers=measurement

C) Output characteristics

$I_d$ vs. $V_{ds}$ ($V_{gs}$ parameter) measurement and simulation are shown in fig. 9 and fig. 10 for PMOS transistor $w/l = 120/6$ junction and ohmic side.

Simulation agrees quite satisfactorily with measurement. Note the high slope in the saturation region; this behaviour is due to the DIBL (Drain-Induced Barrier Lowering) effect [5]: the threshold voltage is a decreasing function of $V_{ds}$ and $I_d$, in the saturation region, will not saturate. Note also the difference in output conductance between devices fabricated on the two sides of the wafer. This is due to a different series resistance of source and drain regions, as measured by means of Van der Paw structures (see table I). The higher $p^+$ implant resistance on the ohmic side causes the lowering of output current with respect to the junction side PMOS devices.
TABLE VI. - μ values for L = 6 μm, L = 4 μm.

<table>
<thead>
<tr>
<th>L (μm)</th>
<th>J-side</th>
<th>Ω-side</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>1.8</td>
<td>3.1</td>
</tr>
<tr>
<td>6</td>
<td>3.6</td>
<td>4.8</td>
</tr>
</tbody>
</table>

D) Small signal parameters

We have extracted the transconductance $g_m$ and output resistance $r_d$ from the output characteristics. In fig. 11 we have $g_m$ for both junction and ohmic sides vs. channel width, measured for a PMOS in saturation region ($V_{gs} = -6$ V, $V_{ds} = -10$ V). Note the linear scaling with the channel width even for narrow channels ($\leq 20$ μm). The different value for $g_m$ on J and Ω sides is due to a different p+ implant dose for drain and source. In table VI the values for $μ = g_m r_d$ at the same operating point are shown, for the two different lengths; $μ$ does not depend on $w$, as expected.

E) Noise measurements

In addition to DC parameters, we have measured the input referred noise of a few PMOS transistors, shown in fig. 12. Given the elevated oxide thickness, the noise spectrum is dominated by the 1/f contribution. At frequencies of interest (beyond 1 MHz) the most significant contribution is due to white noise, which has a value of about 80 nV/√Hz. Assuming to have a 5 cm long transistor (or better as long as a strip), and because of the fact that noise decreases as $1/\sqrt{w}$, we obtain a value of about 4 nV/√Hz, comparable with that of transistors used in commercial amplifier input stages. We are now in the process of optimizing for best S/N the transistor dimensions for a readout system. First indications are that a 50 000/20 strip transistor, coupled to a Viking-like[6] front end, would provide a satisfactory S/N ratio.

Fig. 12. - Noise spectrum PMOS 120/6.
5. - Conclusions

The MOS devices we have realized on high-resistivity silicon are far from being optimal transistors: the DIBL effect causes a low output resistance; the thick gate oxide has bad consequences on the noise figure. Nonetheless these devices have practical applications, their mediocre characteristics being compensated by the huge available area (a typical DSSD is 20–30 cm²). It is for instance possible to realize a large-area MOS whose noise performance and gain would be competitive with high-quality, but small, devices realized with standard CMOS processes.

REFERENCES